Amend

fabrication of said integrated circuit device.

28. (AMENDED) The method according to Claim 21 wherein said inorganic dielectric layer comprises CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen silsesquioxane (HSQ).

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29. (AMENDED) The method according to Claim 26 wherein said organic dielectric layer comprises polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), or organic polymers.

REMARKS

Examiner L. Umez-Eronini is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19, 21, 23, 24, 26, 28, and 29 have been amended.

Claims 1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19, 21, 23, 24, 26, 28, and 29 have been amended to overcome rejection under 35 U.S.C. 112. The Examiner is thanked for her very helpful suggestions in this matter. The confusing terms "first" and "second" have been deleted from the Claims and

Markush language has been corrected. Chemical names for FSG, HSQ, MSQ, and BCB have been provided. The Examiner states that trademark or trade names cannot be properly used to identify material. It is believed that these proprietary materials are commonly identified by their trade names since their chemical makeup is not publicly known. See Exhibit A, attached, in which the low-k dielectric materials claimed in Applicants' claims are identified by their trade names.

All Claims are believed to be in condition for Allowance and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1, 3, 5, 16, 18, and 20 as being unpatentable over Chow in view of Huang et al and Kuo et al is requested in view of Amended Claims 1 and 16 and in accordance with the following remarks.

Claims 1 and 16 detail a via-first dual damascene method as shown in Figs. 1-7. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the Specification). This key feature has been incorporated into Claims 1 and 16 at lines 9-11. Both Chow and Huang et al show the use of etch stop layers. See col. 3, lines 18-23

and Fig. 3 of Chow and col. 6, lines 8-19 and Figs. 5a of Huang et al. In Figs. 5a-5c, Huang et al teaches a via first process, but using an etch stop layer that is eliminated by Applicants' novel invention. It is agreed that Kuo et al teaches that polyimide can be made photosensitive and used as a mask, but this has nothing to do with Applicants' invention.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1, 3, 5, 16, 18, and 20 as being unpatentable over Chow in view of Huang et al and Kuo et al is requested in view of Amended Claims 1 and 16 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 2 and 17 as being unpatentable over Chow in view of Huang et al and Kuo et al and further in view of Joshi et al is requested in view of Amended Claims 1 and 16 and in accordance with the following remarks.

It is agreed that Joshi et al teaches forming semiconductor devices wherein metal lines overlie the devices. However, it is believed that the amendment to Claims 1 and 16 makes it clear that the key feature of Applicants' invention not taught in the prior art is a via

first dual damascene process without an etch stop layer between the two low-k dielectric layers.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 2 and 17 as being unpatentable over Chow in view of Huang et al and Kuo et al and further in view of Joshi et al is requested in view of Amended Claims 1 and 16 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 4 and 18 as being unpatentable over Chow in view of Huang et al and Kuo et al and further in view of Wang et al is requested in view of Amended Claims 1 and 16 and in accordance with the following remarks.

It is agreed that Wang et al teaches forming a dielectric layer that can comprise silicon dioxide or another material such as FSG. However, this layer is used as an etch stop layer in etching an overlying nitride layer (col. 6, lines 65-67) and then as a hard mask for etching the underlying metal layer (col. 8, lines 20-29). This has nothing to do with the low-k dielectric layer of Applicants' invention through which a dual damascene opening is made. Furthermore, it is believed that the amendment to Claims 1 and 16 makes it clear that the key feature of Applicants'

invention not taught in the prior art is a via first dual damascene process without an etch stop layer between the two low-k dielectric layers.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 4 and 18 as being unpatentable over Chow in view of Huang et al and Kuo et al and further in view of Wang et al is requested in view of Amended Claims 1 and 16 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 9, 10, 21, 24, and 25 as being unpatentable over Chow in view of Huang et al is requested in view of Amended Claims 6 and 21 and in accordance with the following remarks.

Claims 6 and 21 detail a trench-first dual damascene method as shown in Figs. 8-13. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the Specification). This key feature has been incorporated into Claims 6 and 21 at lines 9-11. Both Chow and Huang et al show the use of etch stop layers. See col. 3, lines 18-23 and Fig. 3 of Chow and col. 6, lines 48-55 and Fig. 6a of Huang et al. Figs. 6a-6c show a trench first process, but use an etch stop layer not required in

Applicants' novel invention.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 9, 10, 21, 24, and 25 as being unpatentable over Chow in view of Huang et al is requested in view of Amended Claims 6 and 21 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 7 and 22 as being unpatentable over Chow in view of Huang et al and further in view of Joshi et al is requested in view of Amended Claims 6 and 21 and in accordance with the following remarks.

It is agreed that Joshi et al teaches forming semiconductor devices wherein metal lines overlie the devices. However, it is believed that the amendment to Claims 6 and 21 makes it clear that the key feature of Applicants' invention not taught in the prior art is a trench first dual damascene process without an etch stop layer between the two low-k dielectric layers.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 7 and 22 as being unpatentable over Chow in view of Huang et al and further in view of Joshi et al is requested in view of Amended Claims 6 and 21 and in accordance with the

remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 9 and 24 as being unpatentable over Chow in view of Huang et al and further in view of Wang et al is requested in view of Amended Claims 6 and 21 and in accordance with the following remarks.

As discussed above, it is agreed that Wang et al teaches forming a dielectric layer that can comprise silicon dioxide or another material such as FSG. However, this layer is used as an etch stop layer in etching an overlying nitride layer (col. 6, lines 65-67) and then as a hard mask for etching the underlying metal layer (col. 8, lines 20-29). This has nothing to do with the low-k dielectric layer of Applicants' invention through which a dual damascene opening is made. Furthermore, it is believed that the amendment to Claims 6 and 21 makes it clear that the key feature of Applicants' invention not taught in the prior art is a trench first dual damascene process without an etch stop layer between the two low-k dielectric layers.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 9 and 24 as being unpatentable over Chow in view of Huang et al and further in view of Wang et al is requested in

view of Amended Claims 6 and 21 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 11, 13, 15, 26, 29, and 30 as being unpatentable over Chow in view of Huang et al is requested in view of Amended Claims 11 and 26 and in accordance with the following remarks.

Claims 11 and 26 detail a self-aligned dual damascene method as shown in Figs. 14-19. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the Specification). This key feature has been incorporated into Claims 11 and 26 at lines 9-11. Both Chow and Huang et al show the use of etch stop layers. See col. 3, lines 18-23 and Fig. 3 of Chow and col. 8, lines 34-51 and Figs. 8a-8g of Huang et al. Figs. 8a-8g show a self-aligned process, but use an etch stop layer not required in Applicants' novel invention.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 11, 13, 15, 26, 29, and 30 as being unpatentable over Chow in view of Huang et al is requested in view of Amended Claims 11 and 26 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 12 and 27 as being unpatentable over Chow in view of Huang et al and further in view of Joshi et al is requested in view of Amended Claims 11 and 26 and in accordance with the following remarks.

It is agreed that Joshi et al teaches forming semiconductor devices wherein metal lines overlie the devices. However, it is believed that the amendment to Claims 11 and 26 makes it clear that the key feature of Applicants' invention not taught in the prior art is a self-aligned dual damascene process without an etch stop layer between the two low-k dielectric layers.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 12 and 27 as being unpatentable over Chow in view of Huang et al and further in view of Joshi et al is requested in view of Amended Claims 11 and 26 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 14 and 28 as being unpatentable over Chow in view of Huang et al and further in view of Wang et al is requested in view of Amended Claims 11 and 26 and in accordance with the following remarks.

As discussed above, it is agreed that Wang et al teaches forming a dielectric layer that can comprise silicon dioxide or another material such as FSG. However, this layer is used as an etch stop layer in etching an overlying nitride layer (col. 6, lines 65-67) and then as a hard mask for etching the underlying metal layer (col. 8, lines 20-29). This has nothing to do with the low-k dielectric layer of Applicants' invention through which a dual damascene opening is made. Furthermore, it is believed that the amendment to Claims 11 and 26 makes it clear that the key feature of Applicants' invention not taught in the prior art is a self-aligned dual damascene process without an etch stop layer between the two low-k dielectric layers.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 14 and 28 as being unpatentable over Chow in view of Huang et al and further in view of Wang et al is requested in view of Amended Claims 11 and 26 and in accordance with the remarks above.

Applicants have reviewed the prior art not made of record, specifically Huang et al, Zhao et al and Wagganer, and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner Umez-Eronini not find that the Claims are now Allowable that she call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

Rosemary L. S. Pike. Reg # 39,332

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the Claims as follows:

1. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate; depositing [a first] an organic dielectric layer overlying said insulating layer;

depositing [a second] an inorganic dielectric layer overlying said [first] organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a via pattern into said [second] inorganic dielectric layer;

etching said via pattern into said [first] organic dielectric layer using patterned said [second] inorganic dielectric layer as a mask; and

thereafter etching a trench pattern into said [second] inorganic dielectric layer to complete said forming of said dual damascene openings in the

fabrication of said integrated circuit device.

3. (AMENDED) The method according to Claim 1 wherein said [first] organic dielectric layer comprises [one of the group containing:] polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), [and] or organic polymers.

4. (AMENDED) The method according to Claim 1 wherein said [second] inorganic dielectric layer comprises [one of the group containing:] CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, [and] or hydrogen silsesquioxane (HSQ).

6. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing [a first] an organic dielectric layer overlying said insulating layer;

depositing [a second] an inorganic dielectric layer overlying said [first] organic dielectric layer wherein no etch stop layer is formed between said organic

dielectric layer and said inorganic dielectric layer;

etching a trench pattern into said [second] inorganic dielectric layer; and

thereafter etching a via pattern through said [second] inorganic dielectric layer and said [first] organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

8. (AMENDED) The method according to Claim 6 wherein said [first] organic dielectric layer comprises [one of the group containing:] polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), [and] or organic polymers.

9. (AMENDED) The method according to Claim 6 wherein said [second] inorganic dielectric layer comprises [one of the group containing:] CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, [and] or hydrogen silsesquioxane (HSQ).

11. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing [a first] an organic dielectric layer overlying said insulating layer;

depositing [a second] an inorganic dielectric layer overlying said [first] organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a via pattern into said [second] inorganic dielectric layer; and

simultaneously etching said via pattern into said [first] organic dielectric layer and etching a trench pattern into said [second] inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

13. (AMENDED) The method according to Claim 11 wherein said [first] organic dielectric layer comprises [one of the group containing:] polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), [and] or organic polymers.

14. (AMENDED) The method according to Claim 11 wherein said [second] inorganic dielectric layer comprises [one of the group containing:] CORAL, BLACK DIAMOND,

fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, [and] or hydrogen silsesquioxane (HSQ).

16. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing [a first] an inorganic dielectric layer overlying said insulating layer;

depositing [a second] an organic dielectric layer overlying said [first] inorganic dielectric layer wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a via pattern into said [second] organic dielectric layer;

etching said via pattern into said [first] inorganic dielectric layer using patterned said [second] organic dielectric layer as a mask; and

thereafter etching a trench pattern into said [second in]organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

18. (AMENDED) The method according to Claim 16 wherein said [first] inorganic dielectric layer comprises [one of the group containing:] CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, [and] or hydrogen silsesquioxane (HSQ).

19. (AMENDED) The method according to Claim 16 wherein said [second] organic dielectric layer comprises [one of the group containing:] polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), [and] or organic polymers.

21. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing [a first] an inorganic dielectric layer overlying said insulating layer;

depositing [a second] an organic dielectric layer overlying said [first] inorganic dielectric layer wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric

layer;

etching a trench pattern into said [second] organic dielectric layer; and

thereafter etching a via pattern through said [second in]organic dielectric layer and said [first] inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

23. (AMENDED) The method according to Claim 21 wherein said [first] inorganic dielectric layer comprises [one of the group containing:] CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, [and] or hydrogen silsesquioxane (HSQ).

24. (AMENDED) The method according to Claim 21 wherein said [second] organic dielectric layer comprises [one of the group containing:] polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), [and] or organic polymers.

26. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing [a first] an inorganic dielectric layer overlying said insulating layer;

depositing [a second] an organic dielectric layer overlying said [first] inorganic dielectric layer wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a via pattern into said [second] organic dielectric layer; and

simultaneously etching said via pattern into said [first] inorganic dielectric layer and etching a trench pattern into said [second in]organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

28. (AMENDED) The method according to Claim 21 wherein said [first] inorganic dielectric layer comprises [one of the group containing:] CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, [and] or hydrogen silsesquioxane (HSQ).

29. (AMENDED) The method according to Claim 26 wherein said [second] organic dielectric layer comprises [one of the group containing:] polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), [and] or organic polymers.